1.2 kV/25 A Normally-off p-n Junction/AlGaN/GaN HEMTs with Nanosecond Switching Characteristics and Robust Overvoltage Capability

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***Abstract*- With a reverse *p-n* junction in the gate stack design, this work demonstrates a 1.2-kV-class, 25-A normally-off p-n Junction/AlGaN/GaN high electron mobility transistor (PNJ-HEMT) on 6-inch silicon substrate. Benefiting from the robust gate terminal, the PNJ-HEMT exhibits a large gate breakdown voltage of 18.2 V and a positive threshold voltage of 1.7 V, enabling a wide gate-bias window. Thereafter, with an applicable V_{GS} of 10 V, the transient switching characteristics in nanosecond timescale (12.5-ns rise time and 11.0-ns fall time) and notable immunity to dynamic R_{on} degradation, as well as high dynamic breakdown voltage (1.62 kV) under transient overvoltage have been demonstrated. In particular, rugged reliability is validated after the 1-million dynamic breakdown with 1.5 kV peak overvoltage. To the best of our knowledge, this is the first demonstration of high-V_{GS} (10 V) GaN HEMT's operating capability with considerable reliability, and has well exceeded the V_{GS} limit of 5-7 V in conventional *p*-GaN gate-terminal commercial devices, thus possessing great potentials in high-power, high-frequency and high-reliability applications.[1]**

***Index Terms*- GaN, *p-n* junction gate stack, high electron mobility transistor (HEMT), transient switching, dynamic breakdown**

I. Introduction

Robust gate terminal, which is of great significance for protecting the power transistors, determines the critical application requirement to address the false turn-on concern and satisfy the fail-safe operation [1]. In a preferable gate design, its high breakdown voltage ($V_{G\text{-}BV}$) with normally-off characteristics has attracted much interest in recent years, due to a wider safe operation margin and the simplified the gate-driver topology [2], [3]. Considering the inspiring attributes of gallium nitride (GaN) in dealing with high electric field and large current density, rugged gate terminal against breakdown is critical for the safety of device and drivers [4]. In the recent commercial *p*-GaN high-electron-mobility transistors (HEMTs), the gate terminal is either in ohmic or Schottky contact with the *p*-GaN layer [2], allowing a long-term safe operating gate bias of 5~7 V with a limited $V_{G\text{-}BV}$ [2], [5]. Compared with a large operation range of 10-20 V in SiC MOSFETs [6], the narrow gate-bias window of the *p*-GaN HEMTs imposes demanding tasks of suppressing gate ringing, which mainly comes from the parasitic inductance and capacitance in the gate loop [2], [7]. Moreover, low gate voltage headroom has posed significant burden upon gate drive design, while the switching speed is often compromised [5].

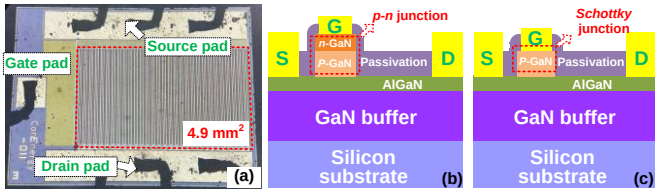

Fig. 1. (a) Optical image and (b) schematic cross-section of the fabricated GaN PHJ-HEMT. (c) Schematic of the SJ-HEMT.

To enlarge the gate-bias window and enhance the gate controllability, a novel *n*-GaN/*p*-GaN/AlGaN/GaN (PNJ) epitaxial structure has been proposed [7], where the Schottky junction is replaced by a reverse *p-n* junction to realize normally-off operation, obtaining a positive V_{TH} of 1.78 V and a high $V_{G\text{-}BV}$ of 19.35 V. Meanwhile, the subsequent comprehensive study on gate current transport mechanisms and long-term gate reliability gain further insights of this advanced device technology [8],[9]. Despite these remarkable results, the effect of the PNJ gate architecture on the dynamic switching behavior of lateral AlGaN/GaN based HEMTs has not yet been investigated, which is indispensable for real applications. When operating in inductive-load dominated converters/inverters power systems, the transient switching capability [10] and dynamic ON-state resistance (R_{on}) degradation phenomenon [11], as well as the overvoltage ruggedness under dynamic breakdown events [12], pose inevitable challenges to the devices, especially for those with newly developed PNJ-gate terminal.

In this work, the feasibility of forming PNJ-gate stack in large-area 1.2 kV/25 A GaN HEMT has been demonstrated, achieving a high $V_{G\text{-}BV}$ of 18.2 V and a remarkably reduced gate leakage current with over 100× lower in magnitude at considerable bias, as compared to conventional Schottky-junction HEMTs. Meanwhile, the required functionality of the PNJ-HEMT has been validated in inductive switching circuits,

This work was supported in part by the National Key R&D Program of China under Grant 2017YFB0403000) and in part by the National Natural Science Foundation of China under Grants 62004099, 61921005 and 91850112. (*Corresponding authors: Weizong Xu; Hai Lu*.)

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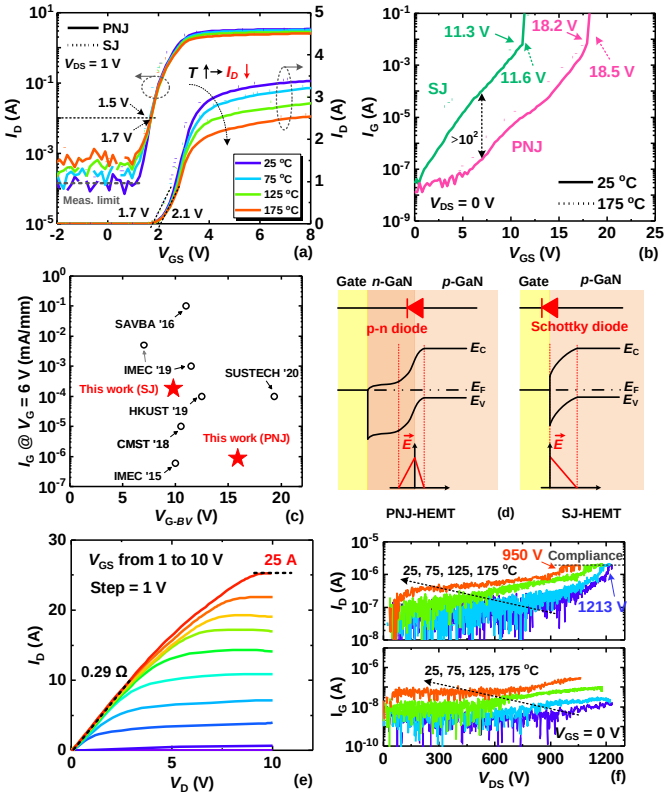

Fig. 2. (a) *T*-dependent Transfer characteristics of the PNJ-HEMT and SJ-HMET in log-scale and linear-scale. (b) I_G-V_{GS} characteristics at 25 °C and 175 °C. (c) Comparison of $V_{G\text{-}BV}$ and I_G with the reported results at 25 °C. (d) Band diagrams and equivalent circuit of the gate region in PNJ-HEMT and SJ-HEMT. (e) Output characteristics and (f) Off-state *I-V* characteristics of the PNJ-HEMT with a floating substrate.

presenting the fast-switching performance and strong immunity to dynamic R_{on} degradation. In particular, the device shows robust overvoltage reliability with a record-high dynamic breakdown voltage (*BV*) of 1.62 kV. This work thus clearly demonstrates the notable potentials of the PNJ-HEMT in high-power, high-speed and high-reliability switching applications.

II. Device Fundamentals

Fig. 1(a) and (b) show the optical image and schematic cross-section view of the GaN PNJ-HEMT grown on a 150-mm Si substrate by metalorganic chemical vapor deposition (MOCVD). The epi layer consists of a 4.5-µm high resistance GaN buffer layer, a 300-nm un-intentionally doped GaN channel, and a 13-nm $Al_{0.2}Ga_{0.8}N$ barrier layer. Meanwhile, the cap layer of the gate stack features a 100-nm p-type GaN layer with Mg-doping concentration of ~2 × 10^{19} cm^{-3} and a 40-nm n-type GaN layer with Si-doping concentration of ~5 × 10^{17} cm^{-3}. It should be noted that the Mg-doping *p*-GaN layer could be passivated by hydrogen from ammonia in the growth of *n*-GaN layer, thus high-temperature activation of *p*-GaN layer is performed after gate pattern definition [9].

The device process begins with the removal of the *n*-GaN and *p*-GaN stack at the access region using low-damage BCl_3/Cl_2-based inductively coupled plasma dry etch, as

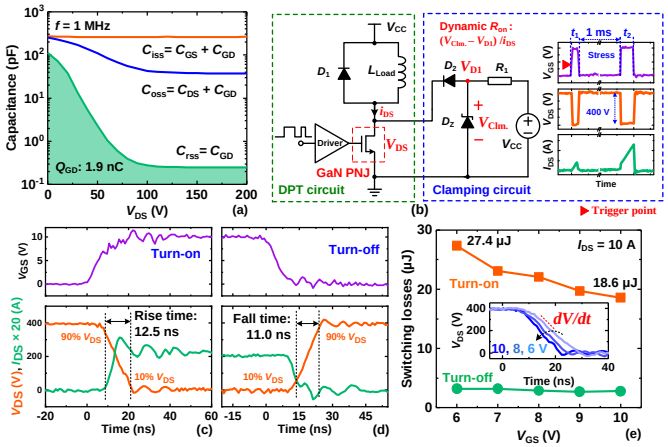

Fig. 3. (a) *C-V* characteristics of the PNJ-HEMT. (b) DPT circuit schematic. The DPT in conjuction with a clamping circuit is used to evaluate dynamic R_{on} characteristics. The inset shows the schematic waveforms and calculation method of the dynamic R_{on}. (c) Turn-on and (d) turn-off switching waveforms at 400 V/10 A. (d) Swithcing losses *vs.* V_{GS}. Inset: Turn-on voltage waveforms at different V_{GS}.

followed by the activation of p-GaN layer at 800 °C for 10 min in N_2 atmosphere [7]. Subsequently, the Ti/Al/TiN metal stack is deposited on the defined gate (G)/source (S)/drain (D) region as the ohmic contact, and annealed with rapid thermal annealing at 600 °C for 2 min in N_2 ambient. Correspondingly, the ohmic contact resistance and sheet resistance of the 2DEG channel are 0.8 Ω·mm and 530 Ω/sq, respectively, as extracted from the transfer length method (TLM) measurements. Finally, a 1-µm-thick SiN_x passivation layer is deposited using plasma-enhanced chemical vapor deposition, followed by dry etching of windows for contact pads and encapsulation in TO-220 packages. As shown in Fig. 1(c), the Schottky-junction HEMT (SJ-HEMT) with a Schottky-type gate metal/p-GaN contact is also fabricated on the same wafer by similar processes for comparison [9]. Both the multi-finger PNJ-HEMTs and SJ-HEMTs feature a gate length of 2.5 µm, a gate width of 90 mm, a gate-source distance of 3 µm and a gate-drain distance of 21 µm, producing an active area of 4.9 mm^2.

III. Results and Discussion

A. Static characteristics

Fig. 2(a) shows the temperature (*T*) dependent transfer characteristics of the PNJ-HEMT and SJ-HEMT measured by a B1505 power device analyzer in the pulsed mode (50-µs pulse width with a duty cycle of 1%). Thanks to the effective *p*-GaN layer activation, the PNJ-HEMT achieves a positive V_{TH} of 1.7 V as extracted at a drain current (I_D) of 10 mA (2.1 V by linear extrapolation). Meanwhile, the V_{TH} of the device shows only minor changes at elevated temperatures (*T*) up to 175 °C, suggesting the good thermal stability of the normally-off operation. The I_D reduces at higher *T*, which should be the result of the decreased carrier mobility with enhanced phonon scattering [9]. Fig. 2(b) shows the *T*-dependent gate breakdown characteristics of the PNJ-HEMT and SJ-HEMT. In comparison with the SJ-HEMT, the $V_{G\text{-}BV}$ has been evidently enhanced from 11.3 V to 18.2 V in PNJ-HEMT at

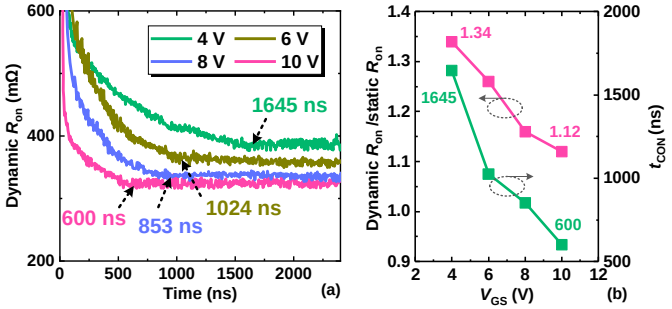

Fig. 4. (a) Time-resolved dynamic R_{on} of PNJ-HEMT with V_{GS} varing from 4 V to 10 V. (b) Dynamic R_{onc}/static R_{on} and t_{CON} as a function of V_{GS}, respectively.

25 °C, featuring a >100× gate leakage reduction at considerable bias. Even at 175 °C, the PNJ-HEMT still shows robust gate controllability with a high $V_{G\text{-}BV}$ of 18.5 V and a small gate leakage (10 μA at V_{GS} = 10 V). These results clearly present the feasibility and reliability of incorporating reverse *p-n* junction in gate stack, being competitive with the state-of-the-art GaN HEMTs (Fig. 2(c)).

Fig. 2(d) shows the schematic band diagrams and equivalent circuit model for the gate structure in PNJ-HEMT and SJ-HEMT, respectively. With the same peak *E*-field, the reverse-biased *p-n* junction could hold a higher voltage than the Schottky junction, owing to the extension of depletion region in the n⁻-GaN gate layer. Meanwhile, considering the higher and thicker barrier under the same forward gate bias, the holes injected from the gate metal could also be reduced by the *p-n* junction [7]. Moreover, the peak *E*-field is buried within the *p-n* junction, and becomes less sensitive to the surface states, as compared to the Schottky junction. Thus, the PNJ-gate has intrinsic advantages over SJ-gate to present a robust gate performance. Additionally, the output and off-state *I-V* characteristics of the PNJ-HEMT are presented in Fig. 2(e) and (f), obtaining a high I_D of 25 A at V_{GS} of 10 V, a low R_{on} of 0.29 Ω and a static *BV* of 1213 V at I_D of 1 μA.

B. Switching and dynamic R_{on} characteristics

Fig. 3(a) shows the *C-V* characteristics of the PNJ-HEMT. Apparently, with the V_{DS} increasing from 0 V to 200 V, the transfer capacitance (C_{rss}) (i.e. gate-to-drain capacitance (C_{GD})) rapidly drops by more than two orders of magnitude, from 200 pF to 0.25 pF. Correspondingly, the Miller charge (Q_{GD}), which strongly affects the rising/falling switching time [13], is as low as 1.9 nC, yielding a low switching figure-of-merit (FOM = R_{on} × Q_{GD}) of 0.55 Ω nC [14], indicating a high-speed switching capability of PNJ-HEMT. As shown in Fig. 3(c) and (d), with an applicable V_{GS} of 10 V, the 400 V/10 A turn-on and turn-off switching waveforms have been presented, respectively, by implementing a double pulse test (DPT) circuit measurement (Fig. 3(b)). The PNJ-HEMT exhibits fast-switching performance with a short rise time/fall time of 12.5 ns/11.0 ns, which is similar to the state-of-the-art GaN transistors [15]. Additionally, for a wide gate-bias window of PNJ-HEMT, the switching losses as a function of V_{GS} has been further investigated (Fig. 3(e)). It can be found that, with an increased V_{GS}, the device exhibits a continuous reduction of

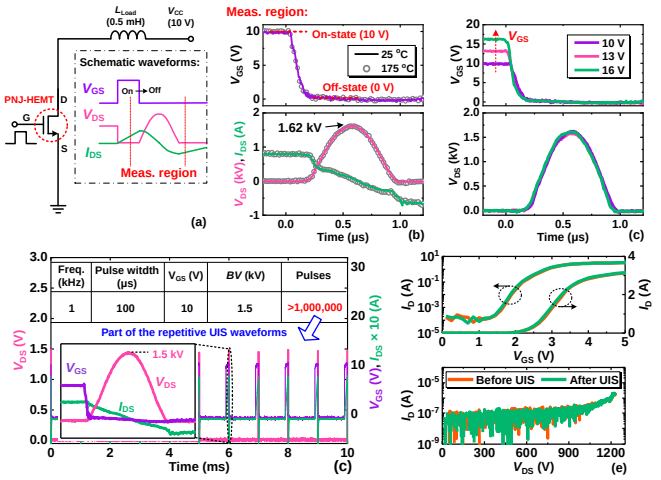

Fig. 5. (a) Schemetic of the UIS circuit and waveforms. (b) *T*-independent dynamic breakdown waveforms corresponding to the measurement region. (c) The dynamic *BV* as a function of V_{GS}. (d) Repetitive UIS waveforms and parameters. (e) Transfer and Off-state *I-V* characteristics of the device before and right after the 1-million UIS pulses with 1.5-kV dynamic *BV*.

turn-on losses from 27.4 μJ to 18.6 μJ. This is because larger V_{GS} leads to a faster channel current building up at the end of turn-off process [16], thus accelerating the device turning on with a high *dV/dt* rate (see the inset in Fig. 3(e)). Moreover, with a high V_{GS} of 10 V, a tolerable gate ringing effect has been observed in PNJ-gate terminal (Fig. 3(c) and (d)). Thus, the V_{GS} of 10 V is applicable in these GaN PNJ-HEMTs for the tradeoff between the gate ringing suppression and the switching loss reduction.

In addition, the DPT configuration with a clamping circuit is developed to characterize the dynamic R_{on} characteristics of the PNJ-HEMT (Fig. 3(b)) [11], [17], where schematic waveforms and extraction method are also illustrated. After determining the trigger starting point at the rising edge of the first 1-μs pulse (t_1), the device is turned off and then stressed with a 400-V high bias for a 1-ms duration. In subsequent second turn-on process (t_2), the dynamic R_{on} with different on-state V_{GS} bias (4 V to 10 V) are measured, as present in Fig. 4(a). Similar to the one reported in [18], the PNJ-HEMT exhibits a strong dependence of dynamic R_{on} on V_{GS}. With V_{GS} increasing from 4 V to 10 V, the dynamic R_{on} is reduced from 388.6 mΩ to 324.8 mΩ, while presenting a shorter conduction time (t_{CON}) to its relatively steady-state level, being reduced from 1645 ns to 600 ns as indicated in Fig. 4(a). Together with the static R_{on} of 290 mΩ, the normalized dynamic R_{on}/static R_{on} and t_{CON} versus on-state V_{GS} are summarized in Fig. 4(b), respectively. As compared with the dynamic R_{on}/static R_{on} ratio of 1.34 at V_{GS} = 4 V, an evidently reduced ratio of 1.12 has been achieved at V_{GS} = 10 V. The smaller dynamic R_{on} and lower t_{CON} should be attributed to the adequate gate over-drive at higher V_{GS} to overcome the V_{TH}-shift-induced dynamic R_{on} degradation [18], while maintaining in the safety operation window of gate bias.

C. Dynamic breakdown ruggedness

In recent studies, the large overvoltage margin with strong gate controllability has been proved to be a critical requirement

for GaN power HEMTs to safely withstand the transient breakdown under hard-switching conditions [12], [19], where otherwise, the device would fail immediately (or with a short delay) and lose all the channel blocking capabilities due to gate failure [12]. Based on the reverse *p-n* junction gate-design, the overvoltage ruggedness of PNJ-HEMT in this work is firstly revealed by employing a widely-used unclamped inductive switching (UIS) test setup. As shown in Fig. 5(a), the load inductor (L_{load}) is firstly charged by the power supply (V_{CC}) with the on-state GaN PNJ-HEMT. Once the device is turned off, the energy stored in the L_{load} is forced to go through the PNJ-HEMT directly, driving it into dynamic breakdown state, whereby the UIS waveforms can be captured by the oscilloscope, with a zoomed-in view of the measurement region shown in Fig. 5(b). Apparently, with a V_{GS} of 10 V, a record-high dynamic *BV* of 1.62 kV is achieved in PNJ-HEMT, which is at least 400 V higher than the static *BV* [12]. Meanwhile, being different from the negative gate-bias-dominated turn-off process as controlled by the additional drivers [12], [19], the PNJ-HEMT exhibits a zero-volt turn-off capability with robust gate control performances. Moreover, the minimal gate ringing with clean gate waveforms has been observed at high temperatures up to 175 ^{o}C. By further widening the gate-bias window to 13-16 V, the PNJ-HEMT retains a comparable dynamic breakdown capability with over 1.5 kV dynamic *BV* (Fig. 5(c)). All these results clearly validate the remarkable gate robustness of the PNJ-HEMT in withstanding the UIS dynamic breakdown events.

In addition to single-pulse UIS event, continuously repeated 1-million UIS pulses are performed with a peak *BV* of 1.5 kV (i.e. 93% of the dynamic *BV*) and a V_{GS} of 10 V to gain further insights of the device ruggedness under dynamic breakdown conditions [20]. As presented in Fig. 5(d), the GaN PNJ-HEMT could survive1 million pulses with almost no changes in the V_{GS} or V_{DS} waveforms. Meanwhile, the static transfer and off-state *I-V* characteristics of the device are measured before and right after these continuous UIS events (Fig. 5(e)), where no noticeable variations could be observed in V_{TH} and *BV*, revealing the negligible degradation in the gate stack and robust dynamic breakdown ruggedness.

IV. Conclusion

In this work, 1.2 kV/25 A normally-off GaN PNJ-HEMT with an *n*-GaN/*p*-GaN gate stack is demonstrated. The device exhibits a large gate breakdown voltage of 18.2 V with a positive V_{TH} of 1.7 V. More importantly, after implementing this device into the inductive-load circuits, fast switching performances with excellent switching figure-of-merit are realized while maintaining a minor dynamic R_{on} degradation, with an applicable V_{GS} of 10 V. In particular, a robust overvoltage capability with a record-high dynamic *BV* of 1.62 kV and 1-million times repeatable breakdown has been demonstrated in the PNJ-HEMT. These results thus present the large potentials of the GaN PNJ-HEMT in high-efficiency, high-power and high-reliability power applications.

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