



CoreGaN 650V GaN HEMT

Description

The CE65H270DNGI Series 650V, 270m Ω gallium nitride (GaN) FETs are normally-off devices.

Coreenergy GaN FETs offer better efficiency through lower gate charge, faster switching speeds, and lower dynamic on-resistance, delivering significant advantages over traditional silicon (Si) devices.

Coreenergy is a leading-edge wide band gap supplier with world-class innovation .

Application

- Adapter
- Renewable energy
- Telecom and data-com
- Servo motors
- Industrial
- Automotive

General Features

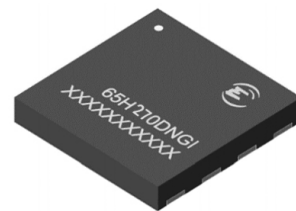
Easy to drive—compatible with standard gate drivers
 Low conduction and switching losses
 RoHS compliant and Halogen-free

Benefits

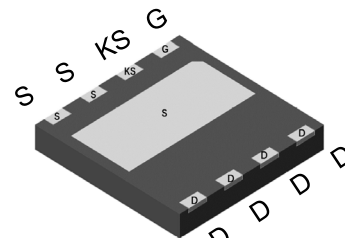
Increased efficiency through fast switching
 Increased power density
 Reduced system size and weight

Ordering Information

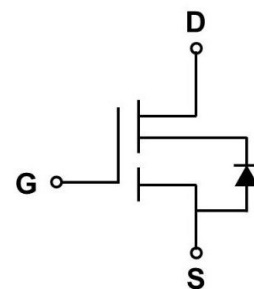
Part Number	Package	Package Configuration
CE65H270DNGI	DFN 8*8	Source



Top



Bottom



Circuit Symbol

Features

BV_{DSS}	$R_{DS(ON)}$	I_{DS}	Q_G
650V	270m Ω	10A	8.5nC



Absolute Maximum Ratings

$T_c=25^\circ\text{C}$ unless otherwise stated

Symbol	Parameter	Limit value	Unit	
V_{DSS}	Drain to source voltage ($T_J = -55^\circ\text{C}$ to 150°C)	650		
$V_{(TR)DSS}$	Drain to source voltage-transient ^a	800	V	
V_{GSS}	Gate to source voltage	-20~+20		
I_D	Continuous drain current @ $T_c=25^\circ\text{C}$ ^b	10	A	
	Continuous drain current @ $T_c=125^\circ\text{C}$ ^b	4.7		
I_{DM}	Pulse drain current (pulse width: 10 μs)	14	A	
P_D	Maximum power dissipation @ $T_c=25^\circ\text{C}$	69	W	
T_C	Operating temperature	Case	-55~150	$^\circ\text{C}$
T_J		Junction	-55~150	$^\circ\text{C}$
T_S	Storage temperature	-55~150	$^\circ\text{C}$	

a. In off-state, spike duty cycle $D < 0.01$, spike duration $< 1\mu\text{s}$

b. For increased stability at high current operation



Thermal Resistance

Symbol	Parameter	Limit value	Unit
$R_{\theta JC}$	Junction-to-case	1.8	$^{\circ}\text{C} / \text{W}$



Electrical Parameters

$T_J=25^\circ\text{C}$ unless otherwise stated

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Forward Device Characteristics						
$V_{(BL)DSS}$	Drain-source voltage	650	-	-	V	$V_{GS}=0V$
$V_{GS(th)}$	Gate threshold voltage	1.2	1.7	2.2	V	$V_{DS}=1V, I_{DS}=1mA$
$\Delta V_{GS(th)}/T_J$	Gate threshold voltage temperature coefficient	-	-7	-	mV/°C	
$R_{DS(on)}$	Drain-source on-resistance	-	270	320	mΩ	$V_{GS}=10V, I_D=1A, T_J=25^\circ\text{C}$
		-	570	-		$V_{GS}=10V, I_D=1A, T_J=150^\circ\text{C}$
I_{DSS}	Drain-to-source leakage current	-	1	10	μA	$V_{DS}=650V, V_{GS}=0V, T_J=25^\circ\text{C}$
		-	5	100		$V_{DS}=650V, V_{GS}=0V, T_J=150^\circ\text{C}$
I_{GSS}	Gate-to-source forward leakage current	-	-	±100	nA	$V_{GS}=\pm 20V$
C_{ISS}	Input capacitance	-	400	-	pF	$V_{GS}=0V, V_{DS}=400V, f=1MHz$
C_{OSS}	Output capacitance	-	16	-		
C_{RSS}	Reverse capacitance	-	1	-		
Q_G	Total gate charge	-	8.5	-	nC	$V_{DS}=400V, V_{GS}=0V \text{ to } 10V, I_D=1A$
Q_{GS}	Gate-source charge	-	0.7	-		
Q_{GD}	Gate-drain charge	-	2.5	-		
Q_{OSS}	Output charge	-	24	-	nC	$V_{GS}=0V, V_{DS}=0V \text{ to } 400V, f=1MHz$
$t_{D(on)}$	Turn-on delay	-	2.5	-	ns	$V_{DS}=400V, V_{GS}=0V \text{ to } 10V, I_D=2.1A,$ $R_{G-on(ext)}=6.8\Omega, R_{G-off(ext)}=2.2\Omega,$ $L=250\mu H$
t_R	Rise time	-	7	-		
$t_{D(off)}$	Turn-off delay	-	9.7	-		
t_F	Fall time	-	28	-		



Electrical Parameters

$T_j=25^\circ\text{C}$ unless otherwise stated

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Reverse Device Characteristics						
V_{SD}	Source-Drain reverse voltage	-	2.3	-	V	$V_{GS}=0\text{V}$, $I_{SD}=5\text{A}$
t_{RR}	Reverse recovery time	-	13	-	ns	$I_F=5\text{A}$, $V_{DD}=400\text{V}$, $dI_F/dt=165\text{A}/\mu\text{s}$
Q_{RR}	Reverse recovery charge	-	3.2	-	nC	



Typical Characteristics

$T_j=25^\circ\text{C}$ unless otherwise stated

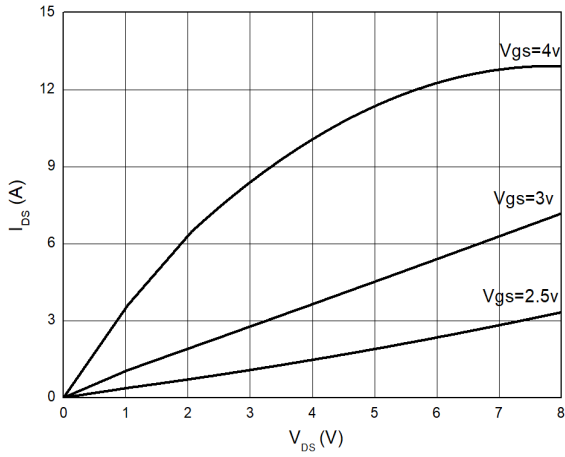


Figure 1. Typical Output Characteristics $T_j=25^\circ\text{C}$

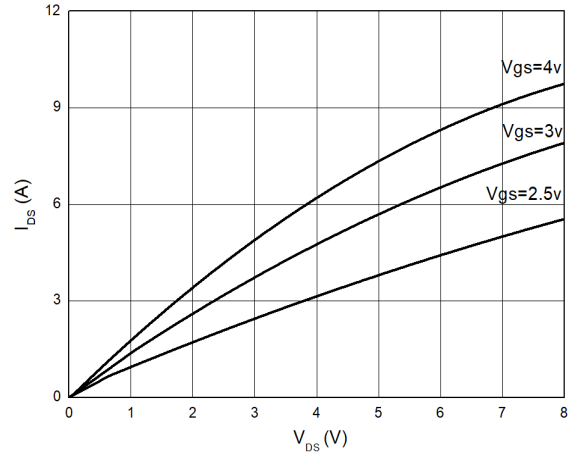


Figure 2. Typical Output Characteristics $T_j=125^\circ\text{C}$

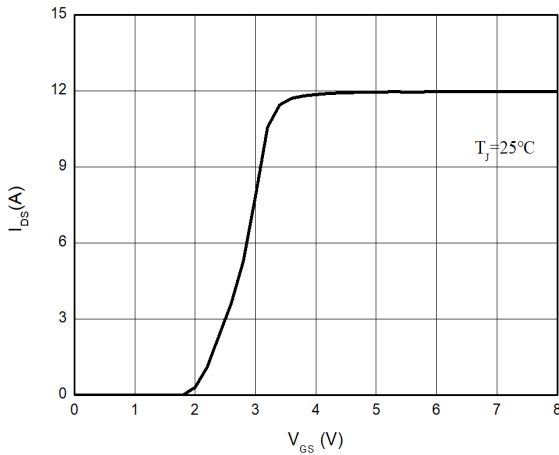


Figure 3. Typical Transfer Characteristics ($V_{bs}=5\text{V}$)

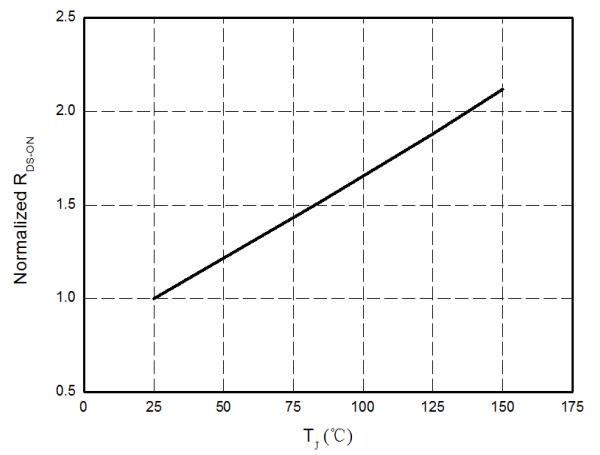


Figure 4. Normalized On-resistance



Typical Characteristics

$T_j = 25^\circ\text{C}$ unless otherwise stated

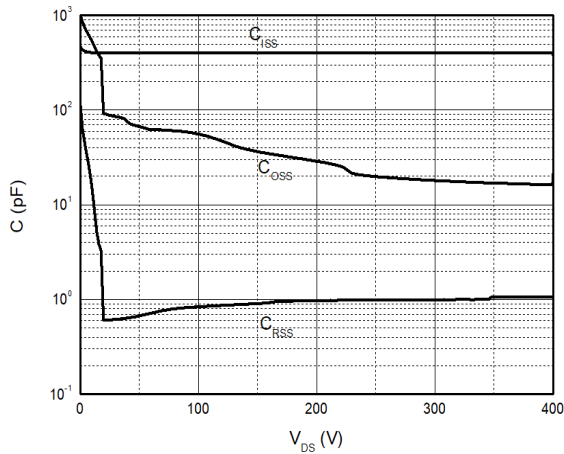


Figure 5. Typical Capacitance (f=1MHz)

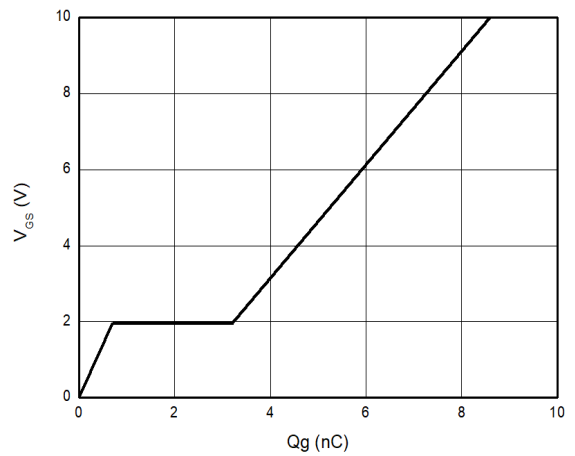


Figure 6. Typical Gate Charge (VDS=400V, ID=1A)

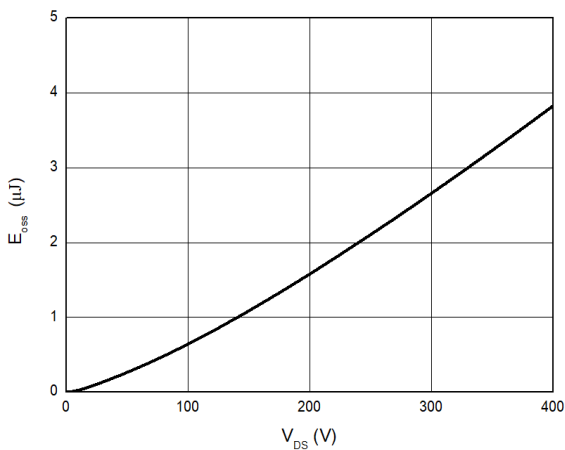


Figure 7. Typical C_{oss} Stored Energy

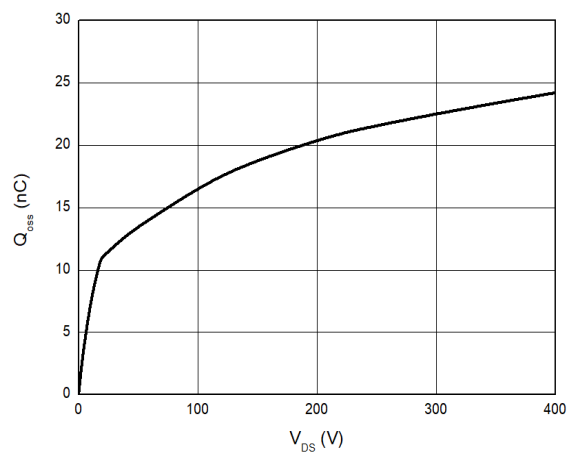


Figure 8. Typical Q_{oss}



Typical Characteristics

T_J=25°C unless otherwise stated

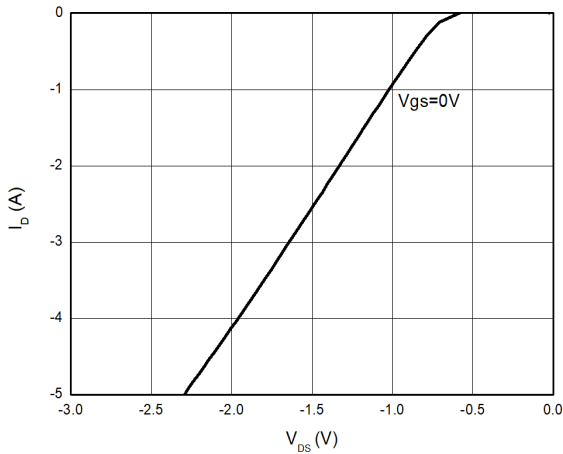


Figure 9. Channel Reverse Characteristics T_J=25°C

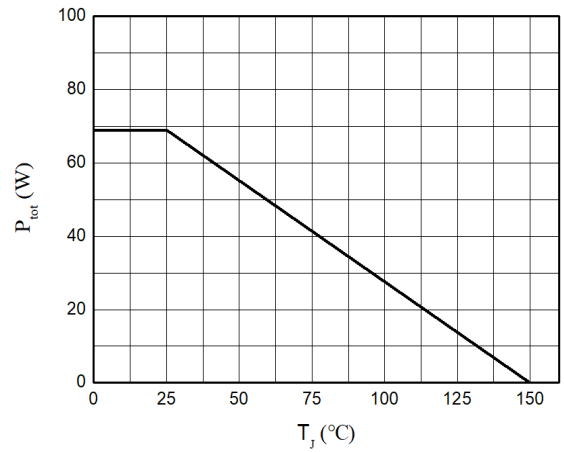


Figure 10. Power Dissipation

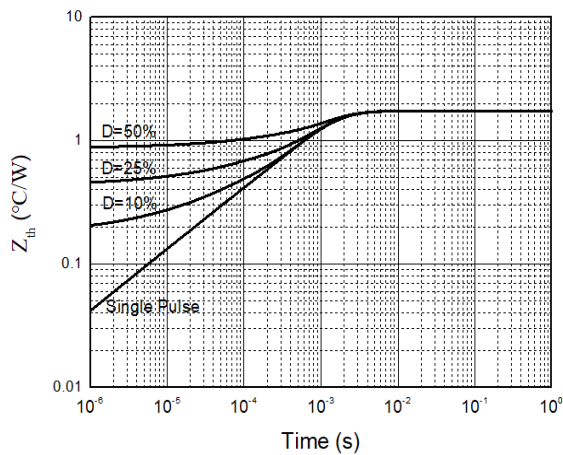


Figure 11. Transient Thermal Resistance

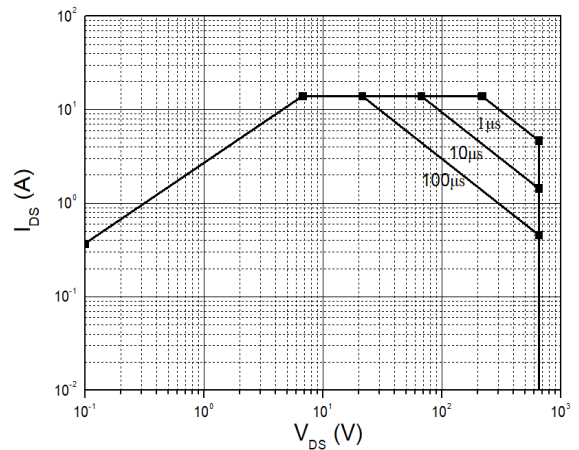


Figure 12. Safe Operating Area T_C=25°C

Typical Characteristics

$T_j=25^\circ\text{C}$ unless otherwise stated

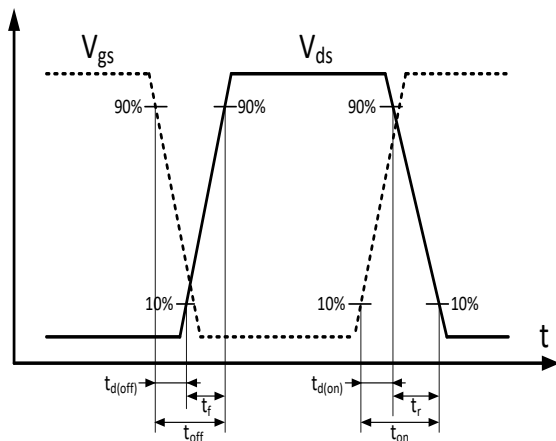


Figure 13. Switching times with waveform

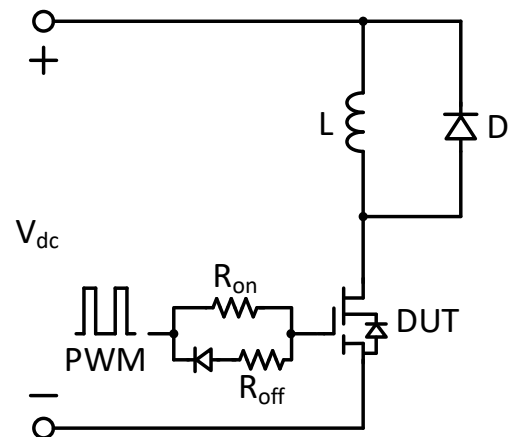


Figure 14. Switching times with inductive load

$V_{DS}=400\text{V}$, $V_{GS}=0\text{V to }10\text{V}$, $I_D=2.1\text{A}$,

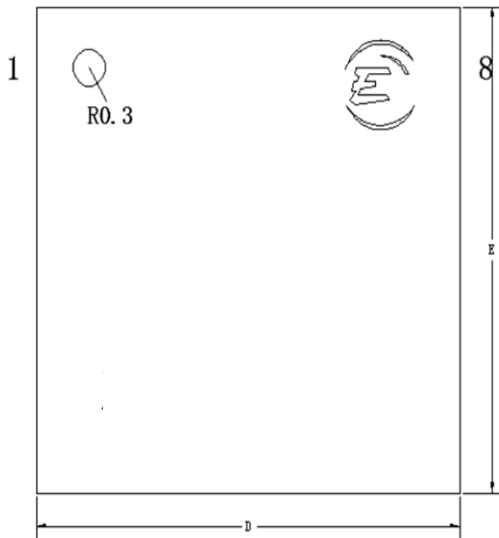
$R_{G-on(ext)}=6.8\Omega$, $R_{G-off(ext)}=2.2\Omega$, $L=250\mu\text{H}$



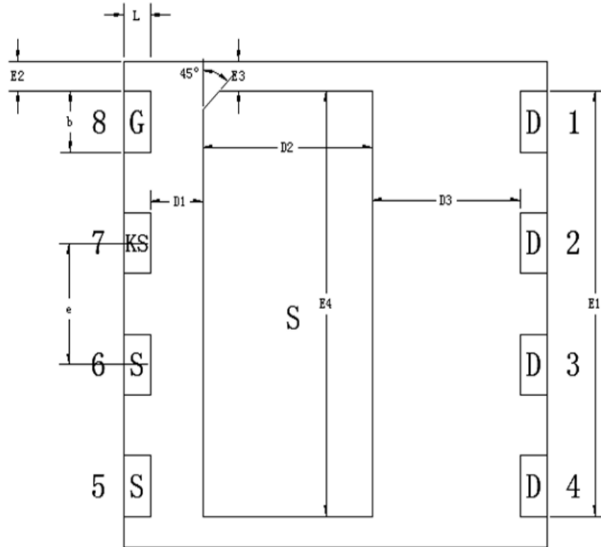
PACKAGE DIMENSIONS

DFN8x8-8L-1.10-A

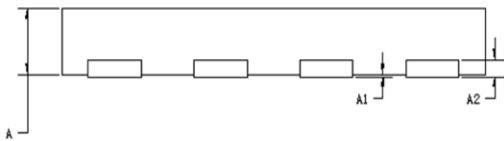
Top view



Bottom view



Side view(left/right)



Symbol	Min. (mm)	Mean. (mm)	Max. (mm)
A	1.05	1.10	1.15
A1	0	0.02	0.05
A2	0.203REF		
D	7.9	8	8.1
E	7.9	8	8.1
D1	0.9	1	1.1
D2	3.1	3.2	3.3
D3	2.7	2.8	2.9
E1	6.9	7	7.1
E2	0.4	0.5	0.6
E3	0.4	0.5	0.6
E4	6.9	7	7.1
e	1.9	2	2.1
b	0.9	1	1.1
L	0.4	0.5	0.6



Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2022-02-28	Initial release
2.0	2023-10-30	Mark change; Enrich dynamic specification curves
3.0	2023-12-25	Update dynamic parameters